Remarks

Thorough examination by the Examiner is noted and appreciated.

The specification has been amended to correct typographical errors.

The claims have been amended to more clearly claim Applicants invention.

Support for the new limitations in amended claims 1 and 13 and new claims 23 and 24 are found in the original claims and the specification at paragraph 0033:

"Following deposition of the I-line photoresist layer 22, an etch back process is carried out to remove the photoresist layer 22 overlying the filled via opening 20 and is further etched through to endpoint detection of the of the metal nitride SiON layer 14. **The etch back is carried out such that at least the via opening 20 adjacent the IMD layer 12 remains filled (plugged) to include covering the via sidewalls to form via plug 24 as shown in Figure 1D.** The etch back process is carried out by a conventional RIE process, with for example an oxygen plasma or a fluorine based chemistry such as CF_4, and CHF_3 with oxygen. The I-line photoresist plug 24 filling via opening 20, acts to reduce the step height in a subsequent trench patterning process thereby improving optical exposure conditions for trench patterning."

The remaining amendments find support in either the original claims or the specification. No new matter has been entered.

Claim Rejections under 35 USC 102(b)

Claims 1-4, 9-16, and 19 stand rejected under 35 USC 102(b) as anticipated by Tobben et al. (US Pat.No. 6,103,456).

Since Examiner refers to claims 5-7, 17-18, and 20 in the same rejection, Applicants assume *arguendo* that these claims stand rejected as well under 35 USC 102(b).

Tobben et al. disclose a method for depositing a dielectric spacer layer over a DARC layer prior to depositing a photoresist layer, patterning and first etching a via opening (see Abstract, Figures 2A-2C, item 42, col 6, lines 20-59). Tobben et al. further teach removing the first photoresist layer and depositing a second photoresist layer to pattern a trench opening followed by etching a trench portion overlying the via opening (see Figures 2D ann 2E, col 7, lines 8-22, col 12, lines 28-47). Tobben et al. teach that following deposition of the second photoresist layer a portion may fill a portion of the via opening

but that this portion is removed in the development process (see col 12, lines 37-40). Tobben et al. further teach that the dielectric space layer is formed of SOG.

Tobben et al. further disclose a prior art process using an organic ARC (col 5, lines 13-63). In the trench etching portion of the prior art process, Tobben et al. disclose that an organic ARC layer is deposited whereby the via opening becomes filled with residual ARC material as well as covering the IMD layer (see e.g., col 8, lines 61 - col 9, lines 1-8, Figure 1D-1E). Tobben et al. then teach that a photoresist layer is deposited over the ARC layer prior to a patterning and etching process (col 5, lines 35-40). Tobben et al. significantly, do not teach removing a portion of the ARC layer to form a via plug, which would defeat the purpose of the ARC layer. Tobben et al. further teach away from the prior art deposition of an organic (resinous) ARC layer due to etching selectivity problems and the formation of ARC material fences (see e.g., col 10, lines 13-26).

Tobben et al. do not teach or disclose Applicants disclosed and claimed invention including the following in amended portions of claims 1 and 13 with respect to the trench forming process:

as in amended claim 1:

"forming a resinous layer over the DARC layer to include filling the via opening;

removing the resinous layer to expose the DARC layer to form a via plug covering at least the dielectric insulating layer portion of the via sidewalls;

forming a photoresist layer over the DARC layer for photolithographically patterning a trench line opening disposed substantially over the via opening;"

forming a photoresist layer over the DARC layer for photolithographically patterning a trench line opening disposed substantially over the via opening;"

and as in amended claim 13:

"forming an I-line photoresist layer over the ~~at least one~~ DARC metal nitride layer to include filling the first opening;

"removing the I-line photoresist layer to expose the DARC metal nitride layer to form a plug filling the first opening at least up to an upper level of the dielectric insulating layer;

forming a DUV photoresist layer over the at least one metal nitride layer for lithographically patterning a second opening disposed over the first opening;"

The disclosure and teachings of Tobben et al. are clearly insufficient to support a rejection under 35 USC 102(b).

With respect to the remaining claims, since the teachings of Tobben et al. do not anticipate Applicants claimed invention with respect to the independent claims, neither are the dependent claims anticipated.

The Claims have been amended to clarify Applicants' invention and newly drafted claims added. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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